Stacking Multiple Differential Pairs for a NEF<1 Amplifier aimed at Electroneurographic Signal Recording

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***Abstract*— A low-noise, electroneurography (ENG) signal recording micro-power amplifier, for a single-channel implantable medical device, is presented. The amplifier is powered by a standard medical grade 3.7V_{nom} secondary battery, and stacks twelve differential pairs maximizing current-reuse and operating them close to saturation with a reduced V_{DS}. The amplifier was implemented in a 0.6µm technology, with a total gain of ~80dB, 200Hz-4kHz bandwidth, and a current consumption of just 16.5µA, with a measured input referred noise of 330nV_{rms} in the band of interest. This result corresponds to a Noise Efficiency Factor NEF=0.84, below the classic limit of 1. On the other hand, the die area of the amplifier is 6mm^2, because very large input transistors and decoupling capacitors are necessary to reduce flicker noise. Thus finally, chopper technique is proposed to reduce flicker noise without resorting to such huge transistors. A new version of the current-reuse amplifier was designed with ~1/80th gate and capacitor area, and almost the same NEF.**

***Index Terms*—current reuse, low-noise, NEF, chopper, autozero**

I. Introduction

NOISE efficiency factor (NEF) defined in [1] is the most widely accepted figure of merit to compare biomedical amplifier designs, having a classical limit of 1 corresponding to the ideal thermal noise of a single BJT.

$$NEF = V_{ni} \cdot \sqrt{I_{Tot}/(2\pi U_T kTB)} \qquad (1)$$

where B, V_{ni}, I_{Tot}, are the amplifier's bandwidth, input referred noise, total current consumption, respectively, $U_T \approx 26$mV is the thermal voltage. The lowest reported NEF values for biomedical amplifiers were achieved using the current reuse technique [2,3,4,12,13] in all cases NEF is above 1. Most current-reuse amplifiers utilize just a complementary differential pair at the input where current from a PMOS differential pair is reused in a second NMOS differential pair. But once the current reuse technique is introduced, the classic NEF > 1 limit is just a milestone without a theoretical support. Recently the first amplifier with a measured NEF lower than 1 was reported in [5], achieved by stacking twelve differential pairs (6 complementary ones) reusing the same supply current. The latter is an electro-neuro-graph (ENG) amplifier for implantable medical devices, aimed at solving a specific problem: to fully exploit the available battery power in a 3.7V_{nom} medical grade lithium secondary battery, without the aid of a DC-DC converter to reduce the supply voltage. It reuses the current from an amplifying pair into another from V_{DD} to *GND* in 12 stages. A scheme is shown in Fig. 1. The amplifier was fabricated in a 0.6µm technology, it has a gain of almost 80dB, 200Hz to 4kHz bandwidth, a measured input referred noise of 330nVrms, CMRR > 60dB, and a total current consumption of only 16.5µA including the biasing circuitry. While the described amplifier exhibits to the authors' knowledge the lowest reported measured NEF, the developed circuit had a too large die area because very large transistors were necessary to make flicker noise contribution negligible. But complementary differential pair stacking is compatible with known circuit techniques to reduce low frequency noise, like autozero or chopper stabilization [6] allowing to drastically reduce the input transistor's and decoupling capacitors size. In this work firstly the amplifier in [5] is revised, providing some extra information. The main criticism that has been made to the circuit is its large area of 6mm^2 which is not compatible with dense multi-channel devices as necessary in some emerging applications. Since huge transistors were placed solely for the sake of reducing flicker noise [7], secondly a chopper version of the 12-pair stacking amplifier is presented including simulation results, reducing almost two orders of magnitude the occupied area while preserving a NEF < 1.

II. A Biomedical Amplifier with a NEF = 0.84

The proposed amplifier has 4 different cascaded stages, but the input stage is the most important, the only one implemented with the stacked pairs technique, consuming 75% of the current budget. A scheme of the amplifier and the input stage stacking six complementary differential pairs are shown in Fig. 1. Each stacked complementary differential pair are named A to F, all of them sharing the same supply current I_{Bias} = 10µA. The input transistors in Fig. 1 are sized $W_{1\text{-}4}/L_{1\text{-}4}$= 2000µm/4µm to operate in weak inversion (WI) and were calculated as large so that the integrated contribution of flicker noise results low in comparison to that of thermal noise in the band of interest. Poly-

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poly decoupling capacitors ($C_{1\text{-}4(A\text{-}F)}$ = 70pF) connect the gate of each input transistor to the inputs V_{IN+} and V_{IN-}. $R_{1(A\text{-}F)}$ and $R_{2(A\text{-}F)}$ are poly resistors of 110kΩ resistance, connected at the output to control the gain and provide a feedback signal for the common mode voltage of each block. The desired middle voltage $V_{M(A\text{-}F)Ref}$ in Fig. 1 is fed to a common mode feedback OTA ($G_{mFB(A\text{-}F)}$) that adjusts $M_{5(A\text{-}F)}$ so that the current through the NMOS and PMOS differential pairs is the same. The G_{mFB}s are standard symmetrical OTAs consuming 125nA each direct from the battery. Note the transistors M_{5i} are not necessarily saturated, and V_{DS5} can be very low e.g., 50mV, thus each complementary differential pair block can operate down to 500mV or less. The simulated gain of this stage is G_1 = 96 V/V (16V/V each of the 6 stacked stages). Stages 2 to 4 are shown in Fig. 2; the second stage is the summing one, adds the 6 differential outputs of the first stage to a single common mode signal V_{O2}, and the two final stages are included to achieve the specified 80dB gain and to further filter the noise outside the band of interest. R_3 = 300kΩ, R_4 =3MΩ, R_5 = 30kΩ, $R_2 = R_6$ = 30MΩ are integrated high resistivity poly resistors, and C_4 = 2pF, C_5 = 340 pF, $C_{sj} = C_2 = C_6$ = 35pF. OA_2, OA_3 and OA_4, are low noise, standard Miller operational amplifiers, consuming a total of 1µA current each directly from the battery. The simulated gains of stages 3, 4 are G_3≈10, G_4≈9.7. The upper 10µA current source is an active one, following the guidelines in [8] to avoid the larger voltage drop of a current mirror and increase its output impedance. Setting the DC bias current of the input transistors in Fig. 1, as well as the correct clamping of the input capacitive divider, are both critical aspects; a detail of a single input transistor bias circuitry is also shown in Fig. 1. Floating diodes are connected to an auxiliary transistor M_{biasN} (M_{biasN} is two hundred times narrower but matched with M_3) that is used to establish an adequate bias voltage at the gate node G_3. The desired source voltage V_{Lrefi} is derived from a 19-tap 10MΩ resistive divider from V_{DD} to *GND*, and M_{biasN} shifts V_{Lrefi} by approximately the V_{GS3} of the input transistor at its nominal 5µA drain current (note M_{biasN} is biased with $1/200^{th}$ of the current of M_3). Approximately a $V_{DD}/6$ voltage room is assigned to each input block from A to F. In Fig. 3 the simulated overall gain of the amplifier is shown, with a typical value G = 9200 V/V. The proposed amplifier was fabricated in a 0.6µm isolated technology and tested; a microphotograph of the ASIC and noise measurement setup are shown in Fig. 4. The measured total supply current consumption of the amplifier including the four stages, references, and auxiliary circuitry is 16.5µA. Fig. 5 shows the measured transfer function of a single circuit sample, and the measured and calculated input referred noise. Because the amplifier is in open loop configuration, the gain G spans from 8000 to 10000 between circuit samples. The measured average -3dB decay frequencies are 200Hz and 4.2kHz, and the measured CMRR was above 60dB in all cases. Note in the input noise plot in Fig. 5 the influence of flicker noise in the PSD. A numerically integrated 330nV_{rms} input referred noise was measured corresponding to a NEF of 0.84.

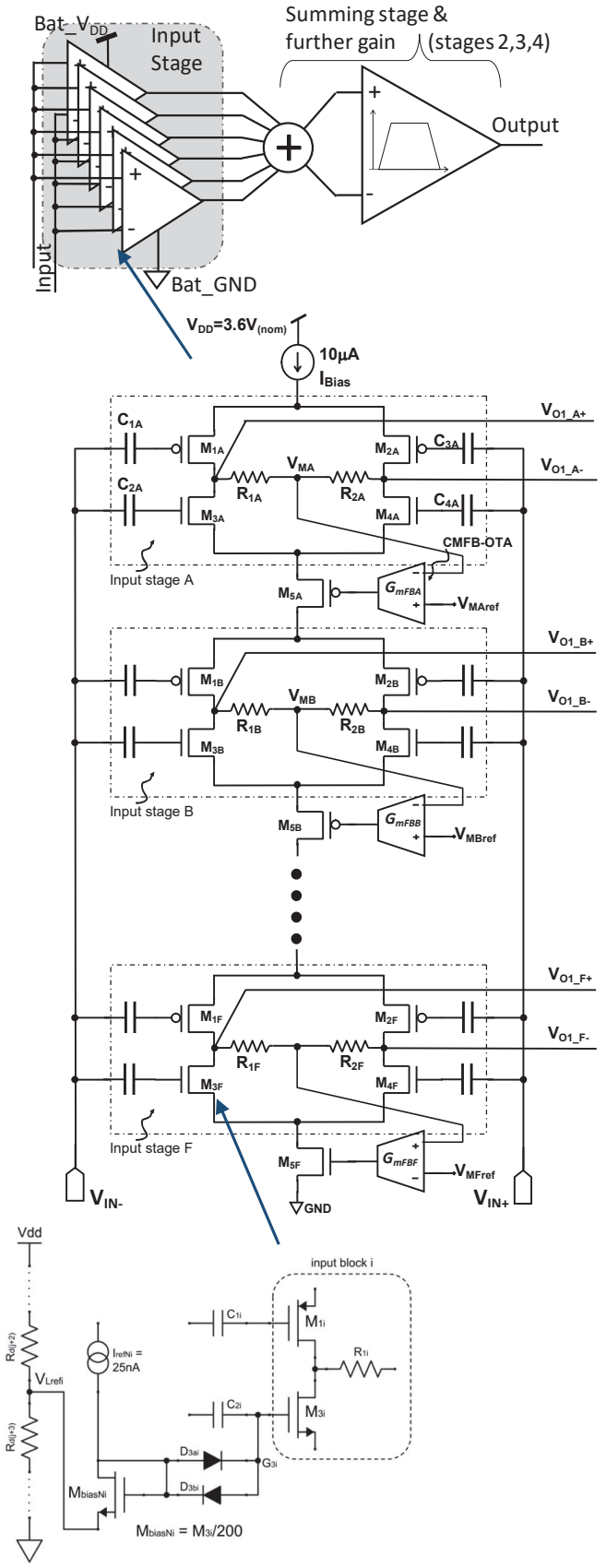

Fig. 1 Block diagram of the proposed ENG amplifier (top), input stage stacking 12 differential pairs reusing the 10µA bias current (middle), and a detail of a single input transistor bias circuitry (bottom). The complementary pairs are grouped in N=6 stages named A to F.

The differential pair stacking technique is very efficient: the 4*N* input transistors amplify the input signal in a cooperative way, but the 4*N* transistors introduce non-correlated noise to the circuit; also most of the energy is dissipated in the input transistors that amplify and not in mirror or bias transistors. In the case of thermal noise, the input referred noise is:

$$S_{Vin}(f) = \frac{\sum S_{Ix}(f)}{(\sum g_{mx}/2)^2} \approx \frac{4N \cdot S_{Ix}(f)}{(2N \cdot g_m)^2} \approx \frac{\gamma nkT}{N g_m} \qquad (2)$$

Where g_m is an input average transconductance, and $S_{Ix}=\gamma nkTg_m$ is the thermal noise current PSD of by each input transistor.

III. Chopper Pair-stacking Amplifier

Very large input transistors were placed in the previous section, calculated to minimize the impact of the integrated flicker noise. But also, very large 70pF input decoupling capacitors are necessary because of the capacitive divider between C_{ij} and the gate-source(drain) parasitic capacitances C_{GSi}, (C_{GDi}), that is also enhanced by the Miller effect [5]. The effective small signal gate voltage of each input transistor is:

$$v_{Gij} = v_{In+(-)} \cdot \frac{C_{ij}}{C_{ij}+C_{GSi}+(G_j-1)C_{GDi}} \ , \qquad (3)$$

$G_j \approx 16$ is the gain of a single complementary pair stage. Thus, a very large C_{ij} = 70pF was necessary so as not to significantly attenuate v_{In} because C_{GSi}, C_{GDi} are too large in a $W_{1\text{-}4}$= 2000µm transistor. To reduce the amplifier's die area, it is possible to introduce either chopper or autozero techniques to reduce flicker noise and lift the restriction of using so large input transistors. The autozero technique was briefly discussed in [11] but because of the inherent noise aliasing [6], it will not allow to reach the lowest NEF. Chopper instead, is essentially a continuous time technique thus is not affected by aliasing. A scheme of the proposed chopper amplifier stacking also 12 differential pairs is shown in Fig. 6. A classic 4-transistor MOS modulator is connected at the input (transistors are sized 20µm/0.6µm) and at the output of each complementary pair, a second (de)modulator changes the sign of the output to the summing stage, resembling the chopper in [10]. These latter output demodulators are either PMOS or NMOS depending on the DC level. The modulating frequency is f_{ch} = 20kHz. The input stage is almost the same in Fig.1 but much smaller $W_{1\text{-}4}/L_{1\text{-}4}$=200µm/1.2µm transistors were selected, as well as only C_i = 1pf decoupling capacitors. Also, apart from the floating diodes, a switched resistor is used to allow the input gate nodes to converge faster to their DC regime voltage. Finally, also the summing stage decoupling capacitors should be drastically reduced. The problem here is to avoid attenuation if C_2 is large, but also C_2-R_2 sets the high pass frequency that shall be low. A solution is provided in Fig. 6 where the resistors R_2 in Fig. 2 where substituted by a MOS pseudo-resistor with an equivalent value in the GΩ order [9]. While this structure can be quite non-linear, its objective is just to set the DC bias of the operational amplifier OA_2 input not substantially affecting the gain.

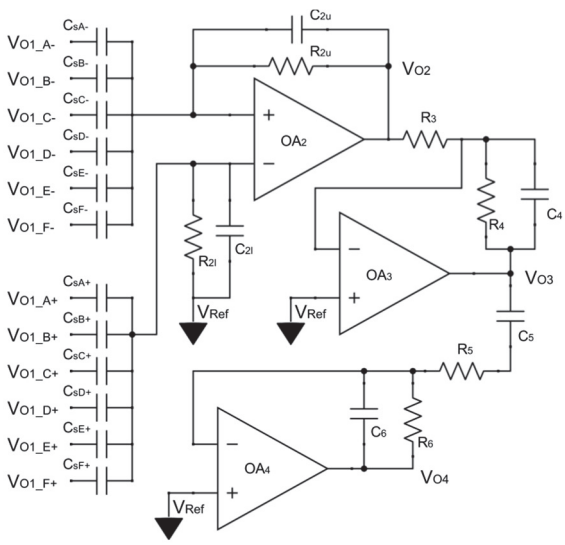

Fig. 2. Stages 2, 3, and 4. Stage 2 adds the 6 outputs of the input stage.

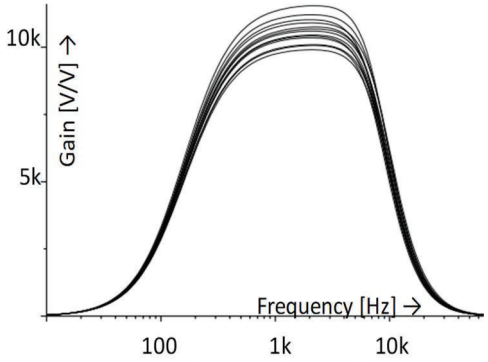

Fig. 3. Montecarlo simulation of the overall gain (4 stages).

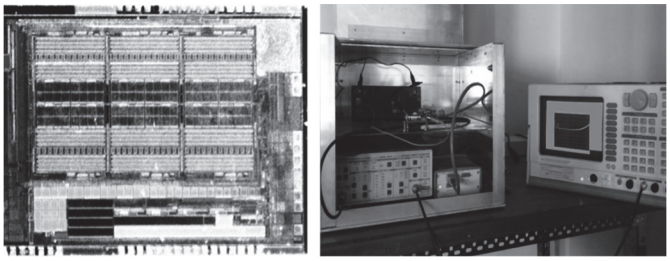

Fig. 4. Microphotograph of the IC (left) and noise measurement setup (right).

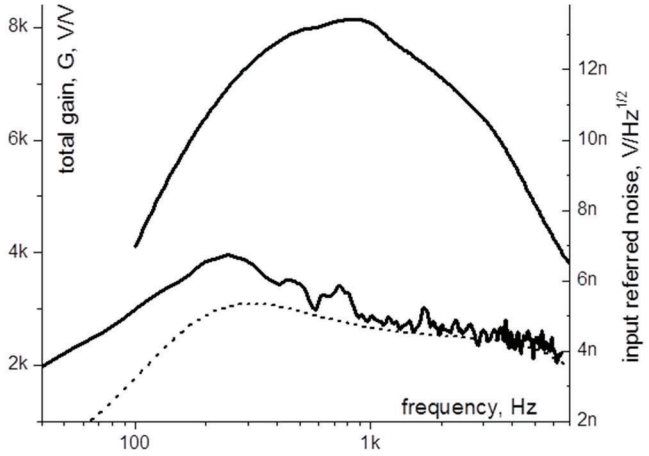

Fig. 5. Measured gain and input referred noise voltage (continuous lines) and calculated input referred noise (dashed line).

IV. Conclusions

In this work, a low-noise ENG signals recording amplifier was presented, it is powered by a $3.7V_{nom}$ battery, and along this supply voltage stacks twelve differential pairs maximizing the supply current reuse. The amplifier was fabricated in an isolated 0.6µm technology and tested, with a measured NEF = 0.84 below the classic limit of 1, a total gain of ~80dB, ~200Hz-4kHz bandwidth, and 16.5µA current consumption. A challenge to overcome is to reduce the die area of the amplifier - $6mm^2$ – without increasing the effect of flicker noise. The chopper technique was proposed to implement a reduced area embodiment of the first amplifier, still stacking 12 differential pairs, but modulating/demodulating the input signal @20kHz to push the flicker noise components out of the band of interest. The new version of the current-reuse amplifier utilizes W/L= 200µm/1.2µm input transistors and C_{ij} = 1pF decoupling capacitors (in comparison to 2000µm/4µm input transistors and 70pF/35pF decoupling capacitors of the first version). The chopper amplifier was simulated, showing no major changes in performance in comparison to the much larger non-modulated version, and almost the same NEF.

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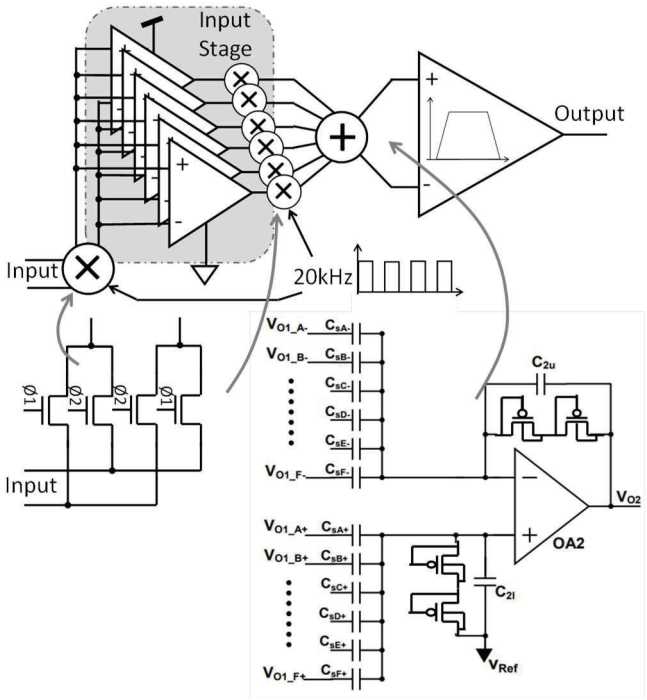

Fig. 6. A scheme of the proposed chopper version of the amplifier in Fig.1.

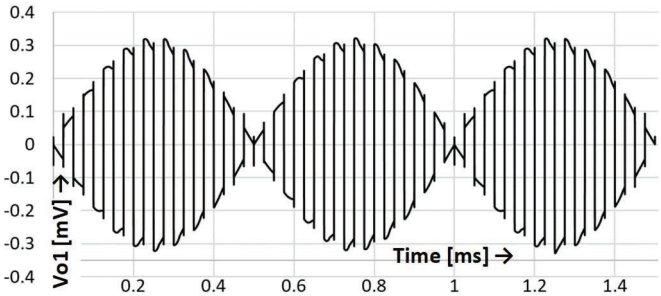

Fig. 7. Transient simulation of the output of a single complementary differential input stage (1 of 6), for 1kkHz,40µV_{pp} input and f_{ch}=20kHz.

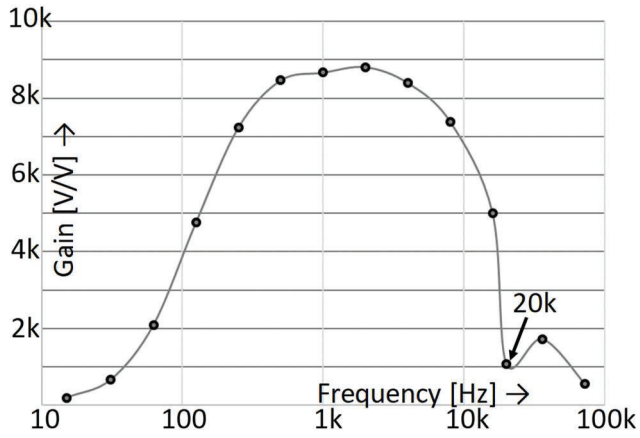

Fig. 8. Simulated transfer function of the chopped version of the amplifier, each point is the result of a transient simulation, and the chopper frequency f_{ch}=20kHz.